

# pqm4: Benchmarking NIST Additional Post-Quantum Signature Schemes on Microcontrollers

Matthias J. Kannwischer<sup>1</sup>, Markus Krausz<sup>2</sup>, Richard Petri<sup>3</sup>, and Shang-Yi Yang<sup>1</sup>

<sup>1</sup> Quantum Safe Migration Center, Chelpis Quantum Tech, Taipei, Taiwan  
matthias@kannwischer.eu, nick.yang@chelpis.com

<sup>2</sup> Horst Görtz Institute for IT Security, Ruhr University Bochum, Bochum, Germany  
markus.krausz@rub.de

<sup>3</sup> Max Planck Institute for Security and Privacy, Bochum, Germany  
rp@rpls.de

**Abstract.** In July 2022, the US National Institute for Standards and Technology (NIST) announced the first set of Post-Quantum Cryptography standards: Kyber, Dilithium, Falcon, and SPHINCS+. Shortly after, NIST published a call for proposals for additional post-quantum signature schemes to complement their initial portfolio. In 2023, 50 submissions were received, and 40 were accepted as round-1 candidates for future standardization.

In this paper, we study the suitability and performance of said candidates on the popular Arm Cortex-M4 microcontroller. We integrate the suitable implementations into the benchmarking framework `pqm4` and provide benchmarking results on the STM32L4R5ZI featuring 640 KB of RAM. `pqm4` currently includes reference implementations for 15 submissions and M4-optimized implementations for five submissions. For the remaining candidates, we describe the reasons that hinder integration – the predominant reason being large key size or excessive memory consumption.

While the performance of reference implementations is rather meaningless and often does not correlate with the performance of well-optimized implementations, this work provides some first indication of which schemes are most promising on microcontrollers. The publicly available implementations in `pqm4` also provide a good starting point for future optimization efforts.

Initially, we were hoping for a much higher code quality than for initial submissions to NIST’s previous PQC project. However, we got grossly disappointed: Half of the submissions make use of dynamic memory allocations, often completely without reason; Many implementations have compiler warnings, sometimes hinting at more serious issues; Many implementations do not pass simple sanitizer tests such as using `valgrind`; Multiple implementations make use of static memory.

## 1 Introduction

While NIST’s initial portfolio of post-quantum cryptography consisting of Kyber [SAB<sup>+</sup>19], Dilithium [LDK<sup>+</sup>19], Falcon [PFH<sup>+</sup>19], and SPHINCS+ [HBD<sup>+</sup>19] provides reasonable performance characteristics for most applications, there are some use-cases that benefit from different trade-offs in terms of key, ciphertext, and signature sizes. Therefore, NIST as well as the cryptography community continues to study schemes achieving different performance characteristics: In Round 4 of the NIST PQC project [NIS23b], there are three code-based key-encapsulation mechanisms (KEMs) with the most prominent candidate being Classic McEliece [BCC<sup>+</sup>22] achieving much smaller ciphertexts than Kyber, but requiring very large public keys. Additionally, NIST [NIS23a] has issued another call for additional post-quantum digital signatures to complement their lattice-based and hash-based signature schemes. The call is primarily for schemes not based on structured lattices, and achieving short signatures and fast verification. By the deadline in June 2023, NIST had received 50 submissions of which they accepted 40 submissions as *complete-and-proper*. These schemes are now being studied in the first round of evaluation.

The first round of evaluation in cryptographic competitions is commonly focussing on the security of the submitted schemes with numerous schemes being broken within hours of appearing publicly [AAS<sup>+</sup>19]. However, as submission teams were required to submit portable C reference implementations as a part of their submission package, we can also evaluate implementation performance and identify any problems with the

---

\* Date of this document: 2024-01-25. `pqm4` version: 62244ef.

submitted implementations. This allows cryptographic engineers to identify promising optimization targets for a wide variety of platforms and publish numerous papers by comparing performance to the reference implementations. The performance of the resulting optimized implementations commonly plays an important role in the selection process beyond round 1 [AASA+20].

Besides the x64 reference platform, NIST is explicitly interested in additional performance results on constrained devices, such as smart cards and microcontrollers. NIST has designated the Arm Cortex-M4 as the primary optimization target in the class of microcontrollers [AASA+20]. During the evaluation of the candidates for the first NIST PQC call, the `pqm4` framework [KRSS19] emerged as the de facto standard evaluation platform for PQC implementations targeting the Arm Cortex-M4 microcontroller. It provides an easy-to-use and automated evaluation framework that unifies benchmarking and implementations of underlying symmetric cryptography to enable fair and meaningful performance comparisons. The `pqm4` repository includes the majority of relevant and publicly available implementations optimized for the Cortex-M4 of selected and remaining PQC candidates from the first NIST call.

In this paper, we extend this repository and evaluate *all* 40 additional signature candidates in terms of their suitability for embedded devices and provide benchmarks for multiple performance characteristics. We extended `pqm4` with 15 reference implementations and five optimized implementations. For the remaining schemes there are either publicly announced severe vulnerabilities, current implementations require too much memory to be functional on any Arm Cortex-M4 platform, or would require major engineering effort to allow porting to `pqm4` and embedded devices in general.

In Section 2 we briefly introduce the `pqm4` framework and the major changes since the first report [KRSS19]. Following, in Section 3 we list the implementations added to `pqm4` or the reasons that prohibit us from doing so for each of the 40 schemes. The performance results can be found in Section 4.

## 2 `pqm4`

The `pqm4` project is a reference framework for benchmarking implementations of PQC KEM and signature schemes for Arm Cortex-M4 based embedded systems. The goal is not just to provide a common ground for comparing the various PQC schemes, but also different implementations of a single scheme. To that end, a set of tests are used to determine performance criteria important to embedded platforms of the basic operations of each scheme: key generation, de- and encapsulation for KEM schemes, or signature generation and verification for signature schemes. The performance criteria covered here are the speed in terms of CPU cycles spent on the operations, as well as static- and dynamic memory usage. Furthermore, a profiling test is used to determine the cycles spent on symmetric primitives, which many schemes use for hashing or as PRNGs for sampling uniformly random bits. The memory usage is analyzed in terms of code size, static memory used, for example, as look-up-tables, and stack-usage during execution. Aside from these performance tests, the framework also includes functional tests, which check the expected behavior of the implementations' APIs. This covers normal functional tests, tests against invalid inputs (invalid secret key or ciphertext during decryption, or invalid public key during verification), and a testvector test, which checks whether each implementation produces the same outputs as a reference implementation on a host platform.

**History.** The initial framework covered 10 KEM and 3 signature schemes (in multiple security levels for some schemes) of the first round of the NIST PQC standardization process. During this first round, the framework was structured as a monolithic framework, targeting only one Arm Cortex-M4 platform. For the second round, the framework was split up into `pqm4` and `mupq`. The former included only platform specific implementations for the Cortex-M4, while the latter covered platform independent implementations suitable for 32 bit embedded platforms and further integrates implementations from the `pqclean` project [KSSW22]. This split facilitated the creation of `pqm3`<sup>4</sup> and `pqriscv`<sup>5</sup>, which aim to cover Arm Cortex-M3 and RISC-V based embedded platforms. For the third round the build system was overhauled from the ground up to support multiple target boards, with a common build system integrated into `mupq` to be used across `pqm4`, `pqm3`, and `pqriscv`. New target boards supported by `pqm4` allowed the use of more memory on larger microcontrollers, or even the QEMU simulator. The simulated platform enables up to 4 MiB flash- and system memory. Lacking

<sup>4</sup> <https://github.com/mupq/pqm3>

<sup>5</sup> <https://github.com/mupq/pqriscv>

any meaningful time-measurement, the simulator is not useful for performance tests concerning speed, but suitable for all memory measurements and functional tests.

**Measurement methodology.** The main tool used for measuring the cycle counts of the scheme operations is the SYSTICK timer available on Arm Cortex-M4 cores. The “Data Watchpoint and Trace Unit” (DWT) in the core features a 32 bit cycle counter, which is, however, insufficient to measure schemes with runtimes exceeding  $2^{32}$  cycles. While the SYSTICK timer itself only uses a 24 bit counter, it can be used for longer measurements, as overflows are caught and counted by an interrupt service routine to measure an arbitrary number of cycles. For the speed benchmarks, the current cycle count is sampled before and after each scheme operation, and the difference taken as the result. Speed tests are repeated, to estimate a minimum-, average-, and maximum runtime for schemes that use random sampling methods. During the profiling tests, the current cycle count is further sampled on entry and exit from symmetric primitives, and the accumulated sum of cycles spent is noted. All schemes integrated in `pqm4` are adapted to use the same implementation for a set of common symmetric primitives (SHA-2, SHA-3/SHAKE, AES), which are regularly updated to the current state-of-art in terms of speed. For AES, `pqm4` offers a bitsliced constant-time implementation [AP20], as well as a faster variable-time t-table implementation [SS17]. To avoid an impact on the speed measurements by the timings of flash-based code memory, which may differ between manufacturers, the target microcontroller runs at a reduced clock frequency during cycle counting tests. The reduced frequency allows the execution of code without any wait-states, the maximum frequency depends on the microcontroller at hand<sup>6</sup>. The memory benchmarks use the compiler toolchain to determine the static memory usage (code- and static data sizes). To determine the dynamic stack usage during runtime, “stack spraying” is used, i.e., the stack is filled with a pattern and checked up to which size it is modified. As no implementations with dynamic heap memory allocations are integrated into `pqm4`, no measurement of heap usage is necessary.

**Target Platform.** Previous versions of `pqm4` targeted the STM32F4DISCOVERY evaluation board, which featured the STM32F407VG microcontroller. The board was chosen for its affordable price and wide availability, and with its 1 MiB flash and 192 KiB SRAM offered a reasonably high amount of memory. For this report, however, we opted for the Nucleo-L4R5ZI evaluation board, featuring a STM32L4R5ZI microcontroller. With 2 MiB flash and 640 KiB SRAM, this new target platform offers a significant increase in memory resources, enabling us to benchmark more of the new signature schemes. The core clock frequency of the board is lower with 120 MHz compared to 168 MHz, the benchmarking clock frequency is further reduced to 20 MHz from 24 MHz. Both the old and the new platform feature a TRNG which is used as the entropy source (`randombytes()`) for the schemes. Our RNG implementation exhibits identical timing performance on both platforms. The memory layout between the platforms differs significantly. On the STM32F407VG, the 192 KiB is made up of three blocks of SRAM: one 112 KiB block, one 16 KiB block, and a 64 KiB core-coupled block. The core-coupled memory was unused by `pqm4`, the second smaller block was only used for schemes which required the additional memory. This was a deliberate choice, as the second block exhibits different memory timings, taking about 1000 cycles more to read a 4 KiB block of memory. For the new platform, we chose not to avoid any memory blocks. The memory layout of the STM32L4R5ZI consists of three blocks: one 192 KiB, one 64 KiB, and one 384 KiB block. Similar to the old platform, only the first block exhibits the fastest timings. Including the slower blocks affects benchmarking results of schemes relying more heavily on memory reads.

**Choice of schemes.** Not all of the 40 accepted submissions for the first round of additional post-quantum digital signatures are suitable for benchmarking in the context of `pqm4`. The first and foremost criteria for inclusion is the size of the key pair and signature, as they have to fit within the constrained memory resources of the chosen embedded platform. At the time of writing, the benchmarking framework is not setup for partial benchmarking of single operations, e.g., benchmarking signature verification of a signature/public key pair generated on an unconstrained system. Hence, only schemes which fit with an entire key pair and signature can be tested. The second criteria is the portability of the available implementations for a scheme. Some of the candidates rely heavily on third party libraries such as GMP or FLINT, which cannot be (easily) ported to an embedded system. Some of the other third party dependencies can be easily replaced. For example, we modified implementations to use our SHA-3/SHAKE implementations, when the original implementation was

---

<sup>6</sup> Higher core clock frequencies require the CPU to enter wait states, to wait for the flash memory to respond. In our case up to six clock cycles, resulting in  $2 - 3\times$  higher cycles counts. The effective execution time is, however, amortized by the higher clock speeds.

making use of the eXtended Keccak Code Package<sup>7</sup> or OpenSSL. The last criteria is the absence of dynamic memory allocations, e.g., using the `malloc` function. While heap-based dynamic memory allocation can be implemented on embedded systems, their use is generally avoided in favor of static or stack-based allocations. As such, the `pqm4` framework only includes implementations that use stack-based allocations.

**Porting implementations.** Integrating a scheme implementation into `pqm4` usually follows similar steps. Some scheme authors already provide suitable implementations, which are integrated easily. In all other cases, we used the reference or optimized implementations included in the submissions accepted by NIST as a startoff point. Wherever necessary, the APIs are adapted to use the correct type system. Next, all calls to symmetric primitives are replaced to those provided by `pqm4`. If dynamic memory allocations are present, they are replaced by stack allocations. In some cases this is a simple replacement of a pointer with an array of appropriate size, e.g., if the allocated memory is not returned from the function. In a few cases, it may also involve allocating the memory in the calling function and passing a pointer. Implementations using more complex memory allocations were not ported to the framework. Some implementations used lookup tables that are computed on-the-fly and cached for future calls. As these caches are allocated statically, they break the reentrancy of the implementation, and complicate performance measurement. For that reason, implementations were modified to allocate the lookup tables on the stack and compute them for every invocation of the scheme. Ideally, implementers should only rely on precomputed lookup tables, allocated to flash memory.<sup>8</sup>

When the implementation can be adapted with the previous steps, it is then integrated and tested using the QEMU simulator. Due to the up to 4 MiB of memory available on the simulated `mps2-an386` platform, all but the largest schemes can be functionally tested and the stack-usage estimated. The result is a list of all integrated implementations and their respective memory requirements. Implementations that fit the target platform are then tested on real hardware, checked whether they pass the functional- and testvector tests, and finally benchmarked for their execution speed. For code- and stack-size benchmarks, the simulated results using QEMU can be considered, as they are identical to those gathered from real hardware.

### 3 New signature schemes included in `pqm4`

**Table 1** gives an overview of all schemes submitted to NIST to the call for additional signature schemes. For each scheme, we either list which implementations have been included in `pqm4` (and reference the respective pull requests), or list the reasons why they cannot be included. We exclude 9 schemes against which (convincing) attacks have been publicly announced on the NIST pqforum. Note that we do not aim to provide a complete picture of the state of cryptanalysis, but instead want to focus our engineering efforts on the schemes that are most likely going to advance the next round. For some schemes, the submission teams provided updated versions addressing vulnerabilities. For four schemes the public keys (for all parameter sets) itself are too large to fit into the memory of our target platform (640 KB). For further seven schemes, current implementations use too much memory to fit onto the target platform. Five schemes require external libraries that are not suitable for the Cortex-M4. One schemes does not have portable C-code. 20 out of 40 schemes have reference implementations that make use of dynamic memory allocations. We tried our best to eliminate those dynamic memory allocations and in the vast majority of cases they can be easily replaced by statically-sized buffers or variable-length arrays. Only for MIRA [ABB<sup>+</sup>23c], RYDE [ABB<sup>+</sup>23b], and FAEST [BBdSG<sup>+</sup>23], the dynamic memory allocations were the main reason for exclusion from `pqm4` as eliminating those would require significant rewriting of the implementations. Overall, we currently have reference implementations for 15 schemes and M4-optimized implementations for five schemes in `pqm4`.

In the following we give the details for each scheme.

#### 3.1 Code-based Signatures

- **CROSS** [BBB<sup>+</sup>23b]: The CROSS reference implementation from the submission package has been merged into `pqm4` in #309. For some parameter sets (e.g., `cross-sha3-r-sdpg-1-small`) test vectors are inconsistent between the host and the Cortex-M4 unless the signed message is initialized to 0 at the

<sup>7</sup> <https://github.com/XKCP/XKCP>

<sup>8</sup> Memory marked `const` is allocated to flash on embedded systems, depending on the linker script.

	issue	PR	pqm4		reason(s) for exclusion							params	
			ref	m4f	vuln	pk	mem	not port	ext lib	dyn mem			
CROSS	[BBB <sup>+</sup> 23b]	#265	#309	✓									12/24
Enhanced pqsigRM	[CNL <sup>+</sup> 23]	#270					x				x		0/1
FuLeeca	[RBK <sup>+</sup> 23]	#272				x							0/3
LESS	[BBB <sup>+</sup> 23a]	#278						x			x		0/7
MEDS	[CNP <sup>+</sup> 23]	#280	#324	✓									2/6
Wave	[BCC <sup>+</sup> 23a]	#298					x				x		0/3
SQIsign	[CSSF <sup>+</sup> 23]	#293								x	x		0/3
EagleSign	[SHDS23]	#267				x							0/4
EHTv3 and EHTv4	[SF23]	#268				x					x		0/5
HAETAETAE	[CCD <sup>+</sup> 23b]	#273	#313	✓	✓								3/3
HAWK	[BBD <sup>+</sup> 23]	#274	#305	✓									3/3
HuFu	[YJL <sup>+</sup> 23]	#276					x				x		0/3
Raccoon	[dPEK <sup>+</sup> 23]	#288							x				0/18
SQUIRRELS	[ENST23]	#294					x			x			0/5
Biscuit	[BKPV23]	#264	#314	✓									3/6
MIRA	[ABB <sup>+</sup> 23c]	#281									x		0/6
MiRitH	[ARZV <sup>+</sup> 23]	#282	#315	✓	✓								16/32
MQOM	[FR23]	#283	#322	✓							(x)		2/12
PERK	[ABB <sup>+</sup> 23a]	#284	#318	✓	✓								12/12
RYDE	[ABB <sup>+</sup> 23b]	#289									x		0/6
SDitH	[MFG <sup>+</sup> 23]	#290						x			x		0/12
3WISE	[Rod23a]	#260				x				x			0/3
DME-Sign	[LA23]	#266				x							0/3
HPPC	[Rod23b]	#275								x			0/3
MAYO	[BCC <sup>+</sup> 23b]	#279	#302	✓	✓								3/4
PROV	[GCF <sup>+</sup> 23]	#286						x			x		0/3
QR-UOV	[FIH <sup>+</sup> 23]	#287						x			x		0/12
SNOVA	[WCD <sup>+</sup> 23]	#291	#311	✓									7/18
TUOV	[DGG <sup>+</sup> 23]	#295	#327	✓				x			x		0/12
UOV	[BCD <sup>+</sup> 23]	#296	#300	✓	✓								3/12
VOX	[PCF <sup>+</sup> 23]	#297				x					x		0/3
AIMer	[KCC <sup>+</sup> 23]	#261	#323	✓							(x)		3/12
Ascon-Sign	[SGJ <sup>+</sup> 23]	#263	#308	✓									8/8
FAEST	[BBdSG <sup>+</sup> 23]	#271									x		0/12
SPHINCS-alpha	[YCZ23]	#292	#312	✓									6/24
ALTEQ	[BDN <sup>+</sup> 23]	#262						x			x		0/6
eMLE-Sig 2.0	[LZ23]	#269				x					x		0/3
KAZ-SIGN	[AAC <sup>+</sup> 23]	#277				x				x	x		0/3
Preon	[CCC <sup>+</sup> 23]	#285						x			x		0/9
Xifrat1-Sign.I	[NP23]	#299				x							0/1
					15	5	9	4	7	1	5	20	83/325

**Table 1.** Overview of the 40 candidates submitted to the NIST call for additional signatures and their status of inclusion in pqm4. Reasons for exclusion include publicly announced severe vulnerabilities, public key sizes exceeding the RAM size of the target device (640 KB), implementations exceeding 640 KB of memory, non-portable code, external dependencies incompatible with the Cortex-M4, and dynamic memory allocations. The last column gives the number of parameter sets for which reference implementations have been integrated into pqm4 and that are functional with 640 KB.

beginning of the signing procedure. We added the initialization, but this hints at missing initialization and possibly unused parts of the signature. For both the `sha2` and `sha3` variants, `spdg-1-fast` and the two respective sets with security level 3 and 5 in addition to `spdg-1-small`, `spd-1-fast` and `spd-2-fast` are running on our physical evaluation platform. This makes in total 12 out of the 24 parameter sets.

- **Enhanced pqsigRM** [CNL+23]: The single parameter set of Enhanced pqsigRM (Enh-pqsigRM-613) has public keys of 2.00 MB and signatures of 1 023 bytes. 2 MB exceeds the available memory on our target M4 platform, and we hence do not include Enhanced pqsigRM in pqm4.
- **FuLeeca** [RBK+23]: FuLeeca has been shown vulnerable by Hörmann and van Woerden<sup>9</sup> and the FuLeeca submission team acknowledged the vulnerability. At the time, no updated version of FuLeeca is available and we, hence, do not include FuLeeca in pqm4. Additionally, when studying the implementation of FuLeeca, we found that it is incorrectly implementing SHAKE (mixing calls to an incremental and non-incremental API). We reported this problem to the submission team and they published a patch resolving this problem.<sup>10</sup> This fix changes KATs.
- **LESS** [BBB+23a]: The LESS reference implementation makes use of dynamic memory allocations. Additionally, signing and verification require a buffer (of type `normalized_IS_t`) of  $T \cdot K \cdot (N - K)$  bytes totaling 3.1 MB (LESS-1s) to 102 MB (LESS-5b). This is far beyond the reach of any micro-controller and, hence, we cannot include LESS into pqm4. We also noticed that `compute_digest` and `compute_digest_array` do not hash the `tree_salt` (due to passing a too short length to the hash function). This appears to be incompatible with the specification and fixing the issue will result in different KATs.
- **MEDS** [CNP+23]: The MEDS reference implementation from the submission package has been merged into pqm4 in #324. Two (meds13220 and meds55604) of the six parameter sets are running on the Nucleo-L4R5ZI board.
- **Wave** [BCC+23a]: Wave uses public keys of 3.7 MB (Wave822) to 13.6 MB (Wave1644) and, hence, can not be included in pqm4.

### 3.2 Isogeny Signatures

- **SQISign** [CSSF+23]: Currently all available implementations of SQISign make heavy use of dynamic memory allocations. This is, in part, due to variable-sized integer arithmetic. Hence, at the moment, we cannot include SQISign in pqm4. We believe that SQISign without dynamic memory allocations is possible, but requires significant engineering efforts. Preliminary experiments (on x86) using the reference implementation in the submission package show that the total memory (stack + heap) of signing of SQISign-NIST-I is slightly above 300 KB. Verification requires only about 12 KB of memory and uses significantly less dynamic memory. The implementation relies on the GMP library.

### 3.3 Lattice-based Signatures

- **EagleSign** [SHDS23]: EagleSign in the version submitted to NIST has been shown to be vulnerable by Tibouchi.<sup>11</sup> Tibouchi published code practically recovering an EagleSign secret key from a sufficient number of signatures.<sup>12</sup> We do not include EagleSign in pqm4.
- **EHTv3 and EHTv4** [SF23]: Practical attacks against EHT (as submitted to NIST) were presented by both Postlethwaite and van Woerden<sup>13</sup> as well as Ryan and Suhl.<sup>14</sup> We do not include EHTv3 and EHTv4 in pqm4.
- **HAETAETAE** [CCD+23b]: HAETAETAE was merged into pqm4 in #313. We include both the reference implementation<sup>15</sup> (v2.0) and the M4F-optimized version described in [CCD+23a]. However, these implementations are not compatible with the original version submitted to NIST (v1.0). Small increases

<sup>9</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/KvIege2EbuM/m/oPrvAPLaBQAJ>

<sup>10</sup> <https://gitlab.lrz.de/tueisec/fuleeca-signature/-/commit/3fc5835ea2e833efd01830944137a8dc0f4d0e58>

<sup>11</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/zas5PLiBe6A/m/A2KSHtqUAgAJ>

<sup>12</sup> [https://github.com/mti/attack\\_eaglesign](https://github.com/mti/attack_eaglesign)

<sup>13</sup> [https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/mFl\\_5Rq6-RU/m/2511f91LAAAJ](https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/mFl_5Rq6-RU/m/2511f91LAAAJ)

<sup>14</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/bkJKBFq3TDY/m/lTCum6zgBQAJ>

<sup>15</sup> <https://kpqc.cryptolab.co.kr/haetae>

in the signature size, resulting from bug fixes and differences in the encoding and packing to address implementation vulnerabilities demonstrated by Saarinen<sup>16 17</sup> make this version incompatible with the original one. All three parameter sets are able to run on our evaluation platform.

- **HAWK** [BBD<sup>+</sup>23]: The reference implementations of HAWK from the submission package have been merged into `pqm4` in #305 and all three parameter sets are running.
- **HuFu** [YJL<sup>+</sup>23]: HuFu uses public keys of 1 059 KB (security level 1) to 3 573 KB (security level 3). This exceeds the available memory available on our target platform and we, thus, do not include HuFu in `pqm4`.
- **Raccoon** [dPEK<sup>+</sup>23]: The reference implementation of Raccoon is making use of the `__int128` datatype which is not portable to our platform. The Raccoon reference implementation offers the option (`POLYR_Q32`) to switch to 32-bit NTTs (`mod 16515073` and `mod 33292289`) rather than 64-bit NTTs (`mod 16515073 · 33292289`) for better support of 32-bit platforms. However, turning on this option does not eliminate all instances of `__int128`. We have contacted the submission team and learned that a fully portable implementation is work in progress. We cannot include Raccoon in `pqm4` at this moment.
- **SQUIRRELS** [ENST23]: SQUIRRELS requires public keys of 666 KB (`Squirrels-I`) to 2 721 KB (`Squirrels-V`) which is too large for our target platform. Furthermore, the reference implementation of SQUIRRELS depends on multiple external libraries. We do not include SQUIRRELS in `pqm4`.

### 3.4 MPC-in-the-Head Signatures

- **Biscuit** [BKPV23]: The reference implementation of Biscuit from the submission package has been merged into `pqm4` in #314. Of the six parameter sets, three (`biscuit128f`, `biscuit192f`, `biscuit256f`) meet the constraints of our evaluation board.
- **MIRA** [ABB<sup>+</sup>23c]: The MIRA reference implementation makes heavy use of dynamic memory that would have to be eliminated prior to merging it into `pqm4`. MIRA is re-using the same data structures (e.g., `gfqm_vec` or `gf16_mat`) for multiple sizes. This requires significant refactoring for eliminating dynamic memory allocations. We do not include MIRA in `pqm4` for now.
- **MiRitH** [ARZV<sup>+</sup>23]: The MiRitH reference implementation from the official repository<sup>18</sup> has been added to `pqm4` in #315. The MiRitH team also provides an implementation optimized for the Cortex-M4 in the same repository. We have merged the optimized implementation in #325. We have reported multiple small issues with those implementations to the submission team which have been fixed in the official repository by now. All `fast` parameter sets of the non-hypercube variant are functional on our testing platform. From the `hypercube` parameter sets, the `fast` and `short` sets for security level 1 and 3 and `mirith_hypercube_Va_fast` and `mirith_hypercube_Vb_fast` are running.
- **MQOM** [FR23]: The MQOM reference implementation from the submission package has been merged into `pqm4` in #322. We have eliminated a large number of dynamic memory allocations from the reference implementation. Luckily, the vast majority of dynamic memory allocations actually had a static size and could easily be replaced. A small number of variable-sized buffers have been replaced by variable-length arrays (VLAs). Those could be replaced with static buffers of worst-case length. Only the two parameter sets `mqom_cat1_gf251_fast` and `mqom_cat1_gf31_fast` of the 12 available sets are suitable for our evaluation board.
- **PERK** [ABB<sup>+</sup>23a]: The PERK team has contributed a reference implementation and a M4-optimized implementation compatible with the specification (v1.1) in #318. The M4 implementation is presented in [BBB<sup>+</sup>24]. This version is, however, incompatible with the one in the NIST submission package. Also note that compared to the official reference implementation (v1.1), the PERK team has replaced the GMP dependency with standalone arithmetic. All parameter sets are running on our evaluation board.
- **RYDE** [ABB<sup>+</sup>23b]: Similar as MIRA, RYDE uses numerous (>50) dynamic memory allocations re-using the same data-structures for differently sized buffers. Including RYDE into `pqm4` would require significant refactoring effort for removing dynamic memory allocations. We do not include it for now.
- **SDitH** [MFG<sup>+</sup>23]: The SDitH reference implementation makes light use of dynamic memory allocations, but those could be eliminated without too much effort. However, the overall memory footprint ranges from

<sup>16</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/ImcSqGLFdo0/m/G86jtgDtBQAJ>

<sup>17</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/Hq-wRFDbIaU/m/iLZctTiLAgAJ>

<sup>18</sup> [https://github.com/Crypto-TII/mirith\\_nist\\_submission/commit/f27b540b77215dd17b10417726c6c6f7ccd41aa5](https://github.com/Crypto-TII/mirith_nist_submission/commit/f27b540b77215dd17b10417726c6c6f7ccd41aa5)

800 KB (for SDitH-L1-gf256) to 2.5 MB (for SDitH-L5-gf256) which exceeds the available memory of our target platform. Getting SDitH to work on the Cortex-M4 would require a stack-optimized implementation. We do not include SDitH in `pqm4` for now.

### 3.5 Multivariate Signatures

- **3WISE** [**Rod23a**]: Smith-Tone [**ST23**] presented a polynomial time attack on 3WISE, therefore, we did not include 3WISE in `pqm4`. Furthermore, the dependency on the FLINT library currently prevents the reference code from being included in `pqm4`.
- **DME-Sign** [**LA23**]: Briaud, Bros, Perlner, and Smith-Tone<sup>19</sup> presented a key recovery attack on DME-Sign, which has been acknowledged by the DME-Sign team. Thus, we currently do not consider adding DME-Sign to `pqm4`.
- **HPPC** [**Rod23b**]: The reference implementation of HPPC unfortunately depends on the external libraries FLINT and M4RI. These external dependencies prohibit a straightforward integration into `pqm4`.
- **MAYO** [**BCC+23b**]: The MAYO reference implementation from the official repository<sup>20</sup> as well as the M4F-optimized implementation described in [**BCC+23c**] have been merged into `pqm4` in [#302](#). Note that [**BCC+23c**] also proposes a change to the MAYO specification by switching to a nibble representation rather than the bitsliced representation. We merged the bitsliced version that is compatible with the round-1 specification. Only the parameter set for the highest security level does not fit on the evaluation board.
- **PROV** [**GCF+23**]: Even for the smallest parameter set (`PROV-I`), PROV requires more than the available 640 KB for generating a signature. The current implementation requires 428 536 bytes for the expanded public key which together with the compressed public key (68 326 bytes) and the secret key (203 688 bytes) already exceeds the available memory.
- **QR-UOV** [**FIH+23**]: QR-UOV has not been included in `pqm4` because the reference implementation allocates huge arrays for signature computation that exceed the available memory resources of our target platform.
- **SNOVA** [**WCD+23**]: We merged the SNOVA reference implementation from the submission package into `pqm4` in [#311](#). The current implementation of SNOVA implementation is using a pre-computed static table `S`. In the reference implementation, this table is computed dynamically and cached. The computation is done outside of the core function and, thus, not reflected in the benchmarks. For a quick integration into `pqm4`, we re-compute this table at the beginning of key generation, signing, and verification, but maintain the static array. This results in fairer benchmarks while not structurally changing the code. A better solution would be to pre-compute the constants and placing them in the code. All three parameter sets targeting security level 1 run both in the `esk` and the `ssk` variant on the evaluation board. `snova-37-8-16-4-ssk` targeting security level three is also running and leading to seven out of 18 variants. [**IA24**] raised concerns about the current SNOVA parameter sets reaching the claimed security levels. The SNOVA team acknowledged these concerns and have proposed updated parameters<sup>21</sup>. However, as of now, no updated implementation is available.
- **TUOV** [**DGG+23**]: The high memory usage of the reference implementation from the submission package of TUOV prevents it from running on our evaluation platform. The parameter set with the lowest memory consumption (`tuov-Ip`) requires around 750 KB of RAM. The implementation is making use of dynamic memory allocations. However, these can be easily eliminated. We included TUOV in `pqm4` in [#327](#), but none of the parameter sets are functional on the target board.
- **UOV** [**BCD+23**]: The UOV implementation from the official repository as well as the M4F-optimized implementation described in [**BCH+23**] have been merged in [#300](#). Note that only the `uov-Ip` parameter sets fit on our target platform. In the paper, the authors are also able to evaluate the `uov-Is` parameters on the same target by writing public and secret keys to flash memory. Writing to flash memory is not supported by the `pqm4` framework. The three security level 1 parameter set require less than the 640 KiB SRAM and are thus functional on our board, the remaining nine parameter sets require more than this.

<sup>19</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/aoXpl4TlNh4/m/Eal1YHw0BAAJ>

<sup>20</sup> <https://github.com/PQCMayo/MAYO-C>

<sup>21</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/m11kg20sTyU/m/cLkGIDaiBAAJ>

- **VOX** [PCF+23]: Furue and Ikematsu [FI23] raised concerns that the security of the current VOX parameters has been severely overestimated.<sup>22</sup> The VOX team has acknowledged the attack and proposes new parameters in [MRPC+23]. However, at this time no reference implementations of the new parameter sets have been published and we, hence, do not include VOX in pqm4.

### 3.6 Symmetric-based Signatures

- **AIMer** [KCC+23]: The AIMer reference implementation from the submission package contains a large number of dynamic memory allocations. All of those can be easily converted into stack allocations. We eliminated the dynamic memory allocations and merged AIMer into pqm4 in #323. However, for some of the parameter sets, that these buffers exceed the 4 MiB stack memory available on qemu’s mps2-an386 (or even the 8 MiB default stack size on Linux). We only include parameter sets that we managed to successfully test using qemu. `aimer-l1-param1`, `aimer-l1-param2` and `aimer-l3-param1` are running on our target platform, nine further parameter sets for AIMer are not.
- **Ascon-Sign** [SGJ+23]: We have merged the Ascon-Sign reference implementation from the submission package into pqm4 in #263. Since pqm4 does not support Ascon, we use the Ascon version shipped in the submission package. All parameter sets are running on our evaluation board.
- **FAEST** [BBdSG+23]: The FAEST reference implementation in the submission package uses a large number of dynamic memory allocations (>150). All of the dynamic memory allocations in `faest_aes.c` and `vole.c` can easily be converted into VLAs. They could also be converted to fixed-sized buffers if defining parameters statically. However, some other dynamic memory allocations are harder to eliminate: The structs `vec_com_t`, `vec_com_rec_t`, `tree_t` hold pointers to buffers that have varying size even for a single parameter set. Those would have to be duplicated for each size needed, or alternatively, the worst case size needs to be used potentially increasing the memory footprint. We do not include FAEST in pqm4.
- **SPHINCS-alpha** [Y CZ23]: The SPHINCS-alpha reference implementation from the submission package has been merged into pqm4 in #312. The implementation used static memory that contains a large (280 KB for `sphincs-a-shake-128f`) lookup table that is computed during first use (i.e., key generation) and re-used throughout the computation including signing and verification. This table computation requires significant time (around 15 million clock cycles for `sphincs-a-shake-128f`). As this leads to unfair benchmarking results in signing and verification, we instead compute the table once in the beginning of each of key generation, signing, and verification. We also move the table to the stack. We were able to make 6 out of 24 variants functional for pqm4: 128f, 128s and 192f each in both the `sha2` and the `shake` version.

### 3.7 Other Signatures

- **ALTEQ** [BDN+23]: The ALTEQ implementation available in the NIST submission package makes heavy use of dynamic memory allocations. Additionally, the memory footprint is too large to fit on our target platform (`alteq-shortsig-I` requires around 1 MB, `alteq-balanced-I` requires around 2 MB). We, thus, do not include ALTEQ in pqm4.
- **eMLE-Sig 2.0** [LZ23]: eMLE-Sig 2.0 has been shown vulnerable by Tibouchi.<sup>23</sup> An implementation of the attack is available.<sup>24</sup> We do not include eMLE-Sig 2.0 in pqm4.
- **KAZ-SIGN** [AAC+23]: Bernstein demonstrated a signature forgery attack against KAZ-SIGN,<sup>25</sup> we therefore did not include the scheme in pqm4. The KAZ-SIGN team has published updated versions four times (with the latest iteration being KAZ-SIGN 1.4<sup>26</sup>), each time being broken by Bernstein within one day.
- **Preon** [CCC+23]: The reference implementation of the smallest parameter set of Preon (`Preon128A`) currently requires around 200 MB of memory for signing. Additionally, it has more than 250 dynamic memory allocations. We do not include Preon in pqm4.

<sup>22</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/icHfTrzkfw4/m/Zj7GrnjMAQAJ>

<sup>23</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/zas5PLiBe6A/m/aOnAlT6cAQAJ>

<sup>24</sup> [https://github.com/mti/attack\\_emle](https://github.com/mti/attack_emle)

<sup>25</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/2ljDcgtawFw/m/61PiLt6WAgAJ>

<sup>26</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/jv72ZzYwAZQ/m/ayNzr7U1GQAJ>

- **Xifrat1-Sign.I** [NP23]: Xifrat1-Sign.I was practically broken by Panny<sup>27</sup>. We do not include it.

## 4 Results

In this section we summarize the benchmarking results at the time of writing. As the `pqm4` framework is under constant development, the numbers may change over time. The largest change for now is the use of a new target platform, which produces different results, due to its different memory timings. This change is accompanied by a newer compiler version. At the time of writing, we use the version 13.2 of the GNU C Compiler toolchain provided by Arm<sup>28</sup>. In the future, implementations for the schemes may be replaced by faster versions, or implementations with other goals (e.g., lower memory requirements) are added. The `pqm4` GitHub repository contains continually updated listing of the results.

Table 2 presents the measured execution speed of each implementation in terms of CPU cycles in thousands (i.e., kilocycles). We measured ten executions per scheme and list the average value, with the exception of the `dilithium`, `haetae`, and `hawk` schemes, which were executed 100 times, due to their significant variance in execution time. The table lists the average cycle counts of all executions, with the difference to the minimum and maximum shown in the super- and subscript. The percentage of cycles spent in symmetric primitives is shown in parentheses. As reference, we included numbers for `dilithium` implementing the third round specification.

Table 3 presents the memory requirements of each implementation. Listed are the sizes of the text (i.e., compiled code), data, and BSS sections produced by the implementations source, as well as the required stacksize (measured in KiB) of each operation, excluding the key, message, and signature. While the code/data sizes can be determined statically with the compiler tools, the stack size was determined using the QEMU simulator. As the QEMU simulator produces the same results for the memory metrics as real hardware platforms and provides more resources, it allows us to test more schemes and security levels. Some of the largest schemes, however, are still too big for the simulated platform.

Table 2: Average execution speed for key generation, signature generation, and signature verification for each scheme implementation, as measured on the Nucleo-L4R5ZI evaluation board. Execution speed is shown in thousands of cycles, with the difference to the minimum and maximum shown in the super- and subscript respectively. Cycles spent on symmetric cryptography shown in parentheses.

Scheme	impl.	keygen	sign	verify
dilithium2	clean	1874 <sup>+41</sup> <sub>-35</sub> (62%)	7283 <sup>+13672</sup> <sub>-3962</sub> (37%)	2062 <sup>+0</sup> <sub>-0</sub> (53%)
	m4f	1426 <sup>+40</sup> <sub>-47</sub> (80%)	3815 <sup>+7908</sup> <sub>-2001</sub> (67%)	1417 <sup>+0</sup> <sub>-0</sub> (77%)
dilithium3	clean	3205 <sup>+2</sup> <sub>-1</sub> (65%)	12893 <sup>+52247</sup> <sub>-7796</sub> (40%)	3376 <sup>+0</sup> <sub>-0</sub> (57%)
	m4f	2516 <sup>+1</sup> <sub>-1</sub> (82%)	6374 <sup>+11353</sup> <sub>-3439</sub> (69%)	2411 <sup>+0</sup> <sub>-0</sub> (79%)
dilithium5	clean	5340 <sup>+66</sup> <sub>-53</sub> (67%)	15533 <sup>+35954</sup> <sub>-7581</sub> (45%)	5610 <sup>+0</sup> <sub>-0</sub> (61%)
	m4f	4277 <sup>+41</sup> <sub>-46</sub> (84%)	8473 <sup>+16493</sup> <sub>-3591</sub> (74%)	4185 <sup>+0</sup> <sub>-0</sub> (82%)
haetae2	ref	9265 <sup>+49825</sup> <sub>-7549</sub> (25%)	32068 <sup>+153018</sup> <sub>-25792</sub> (43%)	1154 <sup>+450</sup> <sub>-50</sub> (45%)
	m4f	9184 <sup>+34372</sup> <sub>-7629</sub> (27%)	26104 <sup>+95950</sup> <sub>-21385</sub> (57%)	918 <sup>+0</sup> <sub>-0</sub> (54%)
haetae3	ref	17553 <sup>+59078</sup> <sub>-14530</sub> (30%)	44320 <sup>+116183</sup> <sub>-34537</sub> (43%)	2097 <sup>+890</sup> <sub>-99</sub> (50%)
	m4f	14630 <sup>+63266</sup> <sub>-11877</sub> (33%)	30588 <sup>+159334</sup> <sub>-23135</sub> (57%)	1761 <sup>+0</sup> <sub>-0</sub> (57%)

<sup>27</sup> <https://groups.google.com/a/list.nist.gov/g/pqc-forum/c/9FXtBZKWueA/m/Dojbrt6ZAgAJ>

<sup>28</sup> <https://developer.arm.com/Tools%20and%20Software/GNU%20Toolchain>

Table 2: Average execution speed for key generation, signature generation, and signature verification for each scheme implementation (cont.)

Scheme	impl.	keygen		sign		verify	
haetae5	ref	19940	$\begin{smallmatrix} +84658 \\ -16076 \end{smallmatrix}$ (31%)	55087	$\begin{smallmatrix} +207542 \\ -43097 \end{smallmatrix}$ (44%)	2593	$\begin{smallmatrix} +1186 \\ -132 \end{smallmatrix}$ (54%)
	m4f	19447	$\begin{smallmatrix} +92871 \\ -15916 \end{smallmatrix}$ (34%)	42365	$\begin{smallmatrix} +162129 \\ -33103 \end{smallmatrix}$ (57%)	2324	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (58%)
hawk256	ref	16846	$\begin{smallmatrix} +22553 \\ -5306 \end{smallmatrix}$ (51%)	1116	$\begin{smallmatrix} +1848 \\ -161 \end{smallmatrix}$ (62%)	628	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (11%)
hawk512	ref	53382	$\begin{smallmatrix} +48360 \\ -8110 \end{smallmatrix}$ (12%)	1972	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (49%)	1294	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (9%)
hawk1024	ref	231721	$\begin{smallmatrix} +308765 \\ -47959 \end{smallmatrix}$ (5%)	4310	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (49%)	2782	$\begin{smallmatrix} +2 \\ -2 \end{smallmatrix}$ (8%)
biscuit128f	ref	1055	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (54%)	274072	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (10%)	254371	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (9%)
biscuit192f	ref	1886	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (54%)	765314	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (6%)	713413	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (6%)
biscuit256f	ref	3302	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (54%)	1747188	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (4%)	1678999	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (4%)
mayo1	ref	7977	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (39%)	18005	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (18%)	6294	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (50%)
	m4f	5242	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (60%)	9101	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (35%)	4953	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (63%)
mayo2	ref	18433	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (23%)	23547	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (18%)	5494	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (76%)
	m4f	11918	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (35%)	11980	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (36%)	5130	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (81%)
mayo3	m4f	18947	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (55%)	32477	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (33%)	16853	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (62%)
ov-1p	ref	350784	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (3%)	6479	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	1301	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (1%)
	m4f	139186	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (8%)	2705	$\begin{smallmatrix} +2157 \\ -240 \end{smallmatrix}$ (1%)	994	$\begin{smallmatrix} +3 \\ -15 \end{smallmatrix}$ (1%)
ov-1p-pkc	ref	375130	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (3%)	6924	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	11430	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (80%)
	m4fspeed	175417	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (6%)	2484	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (1%)	11200	$\begin{smallmatrix} +3 \\ -16 \end{smallmatrix}$ (82%)
	m4fstack	175417	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (6%)	2484	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (1%)	12043	$\begin{smallmatrix} +6 \\ -21 \end{smallmatrix}$ (81%)
ov-1p-pkc-sk	ref	375130	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (3%)	241521	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (5%)	12161	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (81%)
	m4fspeed	175417	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (6%)	89193	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (13%)	11987	$\begin{smallmatrix} +4 \\ -13 \end{smallmatrix}$ (82%)
	m4fstack	175417	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (6%)	89193	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (13%)	12037	$\begin{smallmatrix} +12 \\ -33 \end{smallmatrix}$ (82%)
snova-24-5-16-4-esk	ref	24841	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (12%)	139248	$\begin{smallmatrix} +9 \\ -13 \end{smallmatrix}$ (0%)	88454	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (3%)
snova-24-5-16-4-ssk	ref	24772	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (12%)	174091	$\begin{smallmatrix} +125106 \\ -13926 \end{smallmatrix}$ (2%)	88454	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (3%)
snova-25-8-16-3-esk	ref	35281	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (10%)	65183	$\begin{smallmatrix} +10 \\ -10 \end{smallmatrix}$ (0%)	42543	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (8%)
snova-25-8-16-3-ssk	ref	35195	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (10%)	93185	$\begin{smallmatrix} +13 \\ -11 \end{smallmatrix}$ (4%)	42543	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (8%)
snova-28-17-16-2-esk	ref	51178	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (11%)	21283	$\begin{smallmatrix} +11 \\ -15 \end{smallmatrix}$ (0%)	19180	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (28%)
snova-28-17-16-2-ssk	ref	51065	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (11%)	50759	$\begin{smallmatrix} +9 \\ -13 \end{smallmatrix}$ (11%)	19180	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (28%)
snova-37-8-16-4-ssk	ref	122024	$\begin{smallmatrix} +1 \\ -0 \end{smallmatrix}$ (9%)	576130	$\begin{smallmatrix} +387579 \\ -43107 \end{smallmatrix}$ (2%)	335807	$\begin{smallmatrix} +1 \\ -0 \end{smallmatrix}$ (3%)
cross-sha2-r-sdp-1-fast	ref	5615	$\begin{smallmatrix} +36 \\ -25 \end{smallmatrix}$ (90%)	216566	$\begin{smallmatrix} +830 \\ -822 \end{smallmatrix}$ (86%)	142974	$\begin{smallmatrix} +782 \\ -1350 \end{smallmatrix}$ (91%)
cross-sha2-r-sdp-3-fast	ref	8201	$\begin{smallmatrix} +7 \\ -53 \end{smallmatrix}$ (87%)	241882	$\begin{smallmatrix} +166 \\ -65 \end{smallmatrix}$ (80%)	123737	$\begin{smallmatrix} +585 \\ -782 \end{smallmatrix}$ (82%)
cross-sha2-r-sdpg-1-fast	ref	2151	$\begin{smallmatrix} +24 \\ -35 \end{smallmatrix}$ (93%)	116163	$\begin{smallmatrix} +20 \\ -43 \end{smallmatrix}$ (91%)	87579	$\begin{smallmatrix} +373 \\ -365 \end{smallmatrix}$ (92%)
cross-sha2-r-sdpg-1-small	ref	2151	$\begin{smallmatrix} +24 \\ -35 \end{smallmatrix}$ (93%)	391735	$\begin{smallmatrix} +39 \\ -69 \end{smallmatrix}$ (91%)	368474	$\begin{smallmatrix} +379 \\ -658 \end{smallmatrix}$ (93%)

Table 2: Average execution speed for key generation, signature generation, and signature verification for each scheme implementation (cont.)

Scheme	impl.	keygen		sign		verify	
cross-sha2-r-sdpg-3-fast	ref	3049	$\begin{smallmatrix} +6 \\ -52 \end{smallmatrix}$ (90%)	136249	$\begin{smallmatrix} +47 \\ -13 \end{smallmatrix}$ (87%)	84235	$\begin{smallmatrix} +426 \\ -266 \end{smallmatrix}$ (87%)
cross-sha2-r-sdpg-5-fast	ref	4302	$\begin{smallmatrix} +6 \\ -52 \end{smallmatrix}$ (88%)	221766	$\begin{smallmatrix} +56 \\ -65 \end{smallmatrix}$ (83%)	134737	$\begin{smallmatrix} +422 \\ -591 \end{smallmatrix}$ (82%)
cross-sha3-r-sdp-1-fast	ref	968	$\begin{smallmatrix} +11 \\ -4 \end{smallmatrix}$ (67%)	58864	$\begin{smallmatrix} +13 \\ -11 \end{smallmatrix}$ (61%)	30641	$\begin{smallmatrix} +15 \\ -11 \end{smallmatrix}$ (72%)
cross-sha3-r-sdp-3-fast	ref	2195	$\begin{smallmatrix} +10 \\ -4 \end{smallmatrix}$ (68%)	90063	$\begin{smallmatrix} +18 \\ -32 \end{smallmatrix}$ (58%)	48560	$\begin{smallmatrix} +9 \\ -24 \end{smallmatrix}$ (62%)
cross-sha3-r-sdpg-1-fast	ref	290	$\begin{smallmatrix} +8 \\ -2 \end{smallmatrix}$ (72%)	29964	$\begin{smallmatrix} +10 \\ -4 \end{smallmatrix}$ (75%)	20095	$\begin{smallmatrix} +7 \\ -8 \end{smallmatrix}$ (77%)
cross-sha3-r-sdpg-1-small	ref	290	$\begin{smallmatrix} +8 \\ -2 \end{smallmatrix}$ (72%)	102854	$\begin{smallmatrix} +9 \\ -6 \end{smallmatrix}$ (75%)	75138	$\begin{smallmatrix} +16 \\ -8 \end{smallmatrix}$ (78%)
cross-sha3-r-sdpg-3-fast	ref	628	$\begin{smallmatrix} +10 \\ -2 \end{smallmatrix}$ (72%)	43573	$\begin{smallmatrix} +11 \\ -8 \end{smallmatrix}$ (68%)	27513	$\begin{smallmatrix} +10 \\ -7 \end{smallmatrix}$ (69%)
cross-sha3-r-sdpg-5-fast	ref	1146	$\begin{smallmatrix} +8 \\ -4 \end{smallmatrix}$ (71%)	93558	$\begin{smallmatrix} +6 \\ -9 \end{smallmatrix}$ (66%)	59963	$\begin{smallmatrix} +81 \\ -85 \end{smallmatrix}$ (67%)
meds13220	ref	47801	$\begin{smallmatrix} +4 \\ -4 \end{smallmatrix}$ (2%)	1773022	$\begin{smallmatrix} +26 \\ -23 \end{smallmatrix}$ (5%)	1766410	$\begin{smallmatrix} +66 \\ -58 \end{smallmatrix}$ (5%)
meds55604	ref	253604	$\begin{smallmatrix} +8 \\ -18 \end{smallmatrix}$ (2%)	8009980	$\begin{smallmatrix} +43 \\ -115 \end{smallmatrix}$ (3%)	8320807	$\begin{smallmatrix} +52 \\ -96 \end{smallmatrix}$ (3%)
aimer-l1-param1	ref	393	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (72%)	32386	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (47%)	31112	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (47%)
aimer-l1-param2	ref	393	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (72%)	79451	$\begin{smallmatrix} +1 \\ -0 \end{smallmatrix}$ (49%)	78428	$\begin{smallmatrix} +7 \\ -6 \end{smallmatrix}$ (49%)
aimer-l3-param1	ref	981	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (77%)	90954	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (42%)	88351	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (42%)
mqom_cat1_gf251_fast	ref	7790	$\begin{smallmatrix} +6 \\ -10 \end{smallmatrix}$ (74%)	149074	$\begin{smallmatrix} +10 \\ -6 \end{smallmatrix}$ (33%)	136748	$\begin{smallmatrix} +44 \\ -57 \end{smallmatrix}$ (33%)
mqom_cat1_gf31_fast	ref	8473	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (65%)	243805	$\begin{smallmatrix} +31 \\ -15 \end{smallmatrix}$ (20%)	244375	$\begin{smallmatrix} +71 \\ -53 \end{smallmatrix}$ (19%)
mirith_Ia_fast	ref	1304	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (61%)	296733	$\begin{smallmatrix} +2 \\ -2 \end{smallmatrix}$ (10%)	276068	$\begin{smallmatrix} +21 \\ -22 \end{smallmatrix}$ (10%)
mirith_Ib_fast	ref	2515	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (61%)	565780	$\begin{smallmatrix} +4 \\ -2 \end{smallmatrix}$ (7%)	528405	$\begin{smallmatrix} +5 \\ -4 \end{smallmatrix}$ (6%)
mirith_IIIa_fast	ref	3009	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (64%)	891195	$\begin{smallmatrix} +3 \\ -2 \end{smallmatrix}$ (7%)	831720	$\begin{smallmatrix} +22 \\ -15 \end{smallmatrix}$ (7%)
mirith_IIIb_fast	ref	4565	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (65%)	1298812	$\begin{smallmatrix} +2 \\ -3 \end{smallmatrix}$ (5%)	1214256	$\begin{smallmatrix} +14 \\ -22 \end{smallmatrix}$ (5%)
mirith_Va_fast	ref	6255	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (65%)	2373351	$\begin{smallmatrix} +6 \\ -6 \end{smallmatrix}$ (4%)	2233948	$\begin{smallmatrix} +47 \\ -55 \end{smallmatrix}$ (4%)
mirith_Vb_fast	ref	8808	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (65%)	3406389	$\begin{smallmatrix} +4 \\ -4 \end{smallmatrix}$ (3%)	3205121	$\begin{smallmatrix} +46 \\ -67 \end{smallmatrix}$ (3%)
mirith_hypercube_Ia_fast	ref	1304	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (61%)	116967	$\begin{smallmatrix} +35 \\ -16 \end{smallmatrix}$ (27%)	111503	$\begin{smallmatrix} +14 \\ -30 \end{smallmatrix}$ (24%)
	opt	996	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (78%)	58998	$\begin{smallmatrix} +25 \\ -17 \end{smallmatrix}$ (52%)	53603	$\begin{smallmatrix} +17 \\ -21 \end{smallmatrix}$ (49%)
mirith_hypercube_Ia_short	ref	1304	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (61%)	371003	$\begin{smallmatrix} +20 \\ -3 \end{smallmatrix}$ (67%)	364003	$\begin{smallmatrix} +19 \\ -5 \end{smallmatrix}$ (67%)
mirith_hypercube_Ib_fast	ref	2515	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (61%)	205513	$\begin{smallmatrix} +25 \\ -25 \end{smallmatrix}$ (19%)	199773	$\begin{smallmatrix} +5 \\ -7 \end{smallmatrix}$ (17%)
	opt	1880	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (79%)	83818	$\begin{smallmatrix} +36 \\ -19 \end{smallmatrix}$ (45%)	78142	$\begin{smallmatrix} +9 \\ -7 \end{smallmatrix}$ (42%)
mirith_hypercube_Ib_short	ref	2515	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (61%)	447353	$\begin{smallmatrix} +8 \\ -1 \end{smallmatrix}$ (57%)	440282	$\begin{smallmatrix} +21 \\ -3 \end{smallmatrix}$ (57%)
mirith_hypercube_IIIa_fast	ref	3009	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (64%)	323231	$\begin{smallmatrix} +58 \\ -42 \end{smallmatrix}$ (19%)	313484	$\begin{smallmatrix} +16 \\ -22 \end{smallmatrix}$ (17%)
mirith_hypercube_IIIa_short	ref	3009	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (64%)	718710	$\begin{smallmatrix} +15 \\ -3 \end{smallmatrix}$ (55%)	730959	$\begin{smallmatrix} +6 \\ -9 \end{smallmatrix}$ (56%)
mirith_hypercube_IIIb_fast	ref	4565	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (65%)	450968	$\begin{smallmatrix} +24 \\ -36 \end{smallmatrix}$ (14%)	441592	$\begin{smallmatrix} +14 \\ -9 \end{smallmatrix}$ (12%)
mirith_hypercube_IIIb_short	ref	4565	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (65%)	845099	$\begin{smallmatrix} +17 \\ -4 \end{smallmatrix}$ (47%)	860322	$\begin{smallmatrix} +13 \\ -9 \end{smallmatrix}$ (48%)
mirith_hypercube_Va_fast	ref	6255	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (65%)	808047	$\begin{smallmatrix} +140 \\ -99 \end{smallmatrix}$ (13%)	792074	$\begin{smallmatrix} +59 \\ -84 \end{smallmatrix}$ (12%)

Table 2: Average execution speed for key generation, signature generation, and signature verification for each scheme implementation (cont.)

Scheme	impl.	keygen		sign		verify	
mirith_hypercube_Vb_fast	ref	8808	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (65%)	1134255	$\begin{smallmatrix} +113 \\ -75 \end{smallmatrix}$ (11%)	1117091	$\begin{smallmatrix} +19 \\ -34 \end{smallmatrix}$ (10%)
perk-128-fast-3	ref	698	$\begin{smallmatrix} +7 \\ -4 \end{smallmatrix}$ (59%)	217643	$\begin{smallmatrix} +409 \\ -309 \end{smallmatrix}$ (28%)	96371	$\begin{smallmatrix} +1308 \\ -400 \end{smallmatrix}$ (62%)
	m4	595	$\begin{smallmatrix} +4 \\ -7 \end{smallmatrix}$ (69%)	175927	$\begin{smallmatrix} +4141 \\ -4014 \end{smallmatrix}$ (67%)	81048	$\begin{smallmatrix} +511 \\ -272 \end{smallmatrix}$ (72%)
perk-128-fast-5	ref	911	$\begin{smallmatrix} +43 \\ -2 \end{smallmatrix}$ (51%)	215520	$\begin{smallmatrix} +719 \\ -481 \end{smallmatrix}$ (27%)	93954	$\begin{smallmatrix} +1388 \\ -483 \end{smallmatrix}$ (60%)
	m4	733	$\begin{smallmatrix} +28 \\ -2 \end{smallmatrix}$ (63%)	169043	$\begin{smallmatrix} +6630 \\ -4737 \end{smallmatrix}$ (66%)	78118	$\begin{smallmatrix} +509 \\ -438 \end{smallmatrix}$ (71%)
perk-128-short-3	m4	595	$\begin{smallmatrix} +4 \\ -7 \end{smallmatrix}$ (69%)	976147	$\begin{smallmatrix} +41536 \\ -26439 \end{smallmatrix}$ (64%)	477798	$\begin{smallmatrix} +18823 \\ -19046 \end{smallmatrix}$ (65%)
perk-128-short-5	m4	733	$\begin{smallmatrix} +28 \\ -2 \end{smallmatrix}$ (63%)	902935	$\begin{smallmatrix} +44104 \\ -39106 \end{smallmatrix}$ (63%)	445552	$\begin{smallmatrix} +18846 \\ -19329 \end{smallmatrix}$ (64%)
perk-192-fast-3	m4	1422	$\begin{smallmatrix} +43 \\ -5 \end{smallmatrix}$ (73%)	420038	$\begin{smallmatrix} +7735 \\ -7607 \end{smallmatrix}$ (68%)	194755	$\begin{smallmatrix} +1390 \\ -1202 \end{smallmatrix}$ (72%)
perk-192-fast-5	m4	1679	$\begin{smallmatrix} +46 \\ -14 \end{smallmatrix}$ (68%)	400224	$\begin{smallmatrix} +9757 \\ -11504 \end{smallmatrix}$ (67%)	187024	$\begin{smallmatrix} +993 \\ -768 \end{smallmatrix}$ (71%)
perk-192-short-3	m4	1422	$\begin{smallmatrix} +43 \\ -5 \end{smallmatrix}$ (73%)	2405700	$\begin{smallmatrix} +92909 \\ -108003 \end{smallmatrix}$ (63%)	1203963	$\begin{smallmatrix} +29542 \\ -29447 \end{smallmatrix}$ (63%)
perk-192-short-5	m4	1686	$\begin{smallmatrix} +39 \\ -22 \end{smallmatrix}$ (68%)	2222672	$\begin{smallmatrix} +90220 \\ -70349 \end{smallmatrix}$ (62%)	1120718	$\begin{smallmatrix} +23752 \\ -24792 \end{smallmatrix}$ (62%)
perk-256-fast-3	m4	2482	$\begin{smallmatrix} +50 \\ -9 \end{smallmatrix}$ (74%)	872567	$\begin{smallmatrix} +15040 \\ -14028 \end{smallmatrix}$ (70%)	417918	$\begin{smallmatrix} +2037 \\ -2912 \end{smallmatrix}$ (75%)
perk-256-fast-5	m4	2888	$\begin{smallmatrix} +52 \\ -19 \end{smallmatrix}$ (68%)	834202	$\begin{smallmatrix} +18719 \\ -15315 \end{smallmatrix}$ (70%)	398767	$\begin{smallmatrix} +1968 \\ -1190 \end{smallmatrix}$ (74%)
perk-256-short-3	m4	2482	$\begin{smallmatrix} +50 \\ -9 \end{smallmatrix}$ (74%)	5076941	$\begin{smallmatrix} +110828 \\ -61663 \end{smallmatrix}$ (65%)	2650317	$\begin{smallmatrix} +15593 \\ -20683 \end{smallmatrix}$ (65%)
perk-256-short-5	m4	2882	$\begin{smallmatrix} +57 \\ -3 \end{smallmatrix}$ (68%)	4682541	$\begin{smallmatrix} +89928 \\ -119145 \end{smallmatrix}$ (64%)	2454136	$\begin{smallmatrix} +8774 \\ -8640 \end{smallmatrix}$ (64%)
ascon-sign-128f-robust	ref	122506	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	2855798	$\begin{smallmatrix} +1 \\ -0 \end{smallmatrix}$ (0%)	177864	$\begin{smallmatrix} +4568 \\ -3738 \end{smallmatrix}$ (0%)
ascon-sign-128f-simple	ref	69377	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	1629111	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	96768	$\begin{smallmatrix} +5151 \\ -3091 \end{smallmatrix}$ (0%)
ascon-sign-128s-robust	ref	7842367	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	59267553	$\begin{smallmatrix} +14 \\ -16 \end{smallmatrix}$ (0%)	61063	$\begin{smallmatrix} +2616 \\ -4028 \end{smallmatrix}$ (0%)
ascon-sign-128s-simple	ref	4441129	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	33877716	$\begin{smallmatrix} +16 \\ -22 \end{smallmatrix}$ (0%)	34009	$\begin{smallmatrix} +1442 \\ -1534 \end{smallmatrix}$ (0%)
ascon-sign-192f-robust	ref	222614	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	5712961	$\begin{smallmatrix} +3 \\ -2 \end{smallmatrix}$ (0%)	320251	$\begin{smallmatrix} +4393 \\ -4910 \end{smallmatrix}$ (0%)
ascon-sign-192f-simple	ref	128167	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	3345488	$\begin{smallmatrix} +7 \\ -4 \end{smallmatrix}$ (0%)	178458	$\begin{smallmatrix} +10555 \\ -5104 \end{smallmatrix}$ (0%)
ascon-sign-192s-robust	ref	14249839	$\begin{smallmatrix} +1 \\ -2 \end{smallmatrix}$ (0%)	126646611	$\begin{smallmatrix} +24 \\ -19 \end{smallmatrix}$ (0%)	109281	$\begin{smallmatrix} +6202 \\ -7236 \end{smallmatrix}$ (0%)
ascon-sign-192s-simple	ref	8204011	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (0%)	74760764	$\begin{smallmatrix} +23 \\ -38 \end{smallmatrix}$ (0%)	61709	$\begin{smallmatrix} +2204 \\ -1276 \end{smallmatrix}$ (0%)
sphincs-a-sha2-128f	ref	30279	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (43%)	382271	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (87%)	35696	$\begin{smallmatrix} +2 \\ -1 \end{smallmatrix}$ (48%)
sphincs-a-sha2-128s	ref	814837	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (73%)	6981930	$\begin{smallmatrix} +5 \\ -6 \end{smallmatrix}$ (88%)	187091	$\begin{smallmatrix} +2 \\ -3 \end{smallmatrix}$ (12%)
sphincs-a-sha2-192f	ref	45931	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (58%)	634374	$\begin{smallmatrix} +2 \\ -1 \end{smallmatrix}$ (88%)	35146	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (46%)
sphincs-a-shake-128f	ref	61578	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (72%)	1188147	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (96%)	76330	$\begin{smallmatrix} +2 \\ -2 \end{smallmatrix}$ (76%)
sphincs-a-shake-128s	ref	2342299	$\begin{smallmatrix} +1 \\ -2 \end{smallmatrix}$ (91%)	22926755	$\begin{smallmatrix} +4 \\ -3 \end{smallmatrix}$ (97%)	241835	$\begin{smallmatrix} +2 \\ -3 \end{smallmatrix}$ (32%)
sphincs-a-shake-192f	ref	110028	$\begin{smallmatrix} +0 \\ -0 \end{smallmatrix}$ (83%)	1814954	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (97%)	64022	$\begin{smallmatrix} +1 \\ -1 \end{smallmatrix}$ (71%)

Table 3: Memory requirements for each scheme implementation. Code, data and BSS size listed are in bytes, stack usage in  $2^{10}$  byte (i.e., KiB).

Scheme	impl.	library size			stack usage		
		code	data	bss	keygen	sign	verify
dilithium2	clean	7996	0	0	37.4	50.7	35.3
	m4f	18516	0	0	37.4	48.2	35.3
dilithium3	clean	7496	0	0	59.4	77.7	56.3
	m4f	20004	0	0	59.4	67.2	56.3
dilithium5	clean	7784	0	0	95.4	119.7	90.6
	m4f	18312	0	0	95.4	113.2	90.6
haetae2	ref	25568	0	0	25.5	53.1	29.0
	m4f	35708	0	0	19.3	54.3	22.8
haetae3	ref	25980	0	0	42.5	78.5	47.3
	m4f	35936	0	0	28.8	81.4	31.0
haetae5	ref	25688	0	0	53.5	97.8	60.6
	m4f	35692	0	0	33.3	101.4	36.3
hawk256	ref	102015	0	0	7.7	3.2	3.6
hawk512	ref	102027	0	0	14.2	4.7	6.1
hawk1024	ref	102031	0	0	27.2	7.8	11.2
biscuit128f	ref	7580	0	0	0.6	134.0	14.2
biscuit128s	ref	7696	0	0	0.6	1067.6	81.7
biscuit192f	ref	7780	0	0	0.6	259.6	20.2
biscuit192s	ref	7904	0	0	0.6	2193.0	104.7
biscuit256f	ref	8216	0	0	0.7	466.2	32.2
biscuit256s	ref	8248	0	0	0.7	3889.6	144.7
mayo1	ref	26436	8	0	72.7	213.5	390.0
	m4f	19300	8	0	72.7	110.8	430.3
mayo2	ref	24404	8	0	108.9	232.7	263.9
	m4f	17292	8	0	108.9	121.7	271.8
mayo3	ref	30828	8	0	239.0	699.2	1110.7
	m4f	23612	8	0	239.0	332.7	458.8
ov-1p	ref	29215	0	0	15.2	12.4	6.0
	m4f	118939	0	0	15.2	5.1	2.5
ov-1p-pkc	ref	29423	0	0	15.2	12.4	277.9
	m4fspeed	119131	0	0	138.8	5.1	274.4
	m4fstack	119059	0	0	138.8	5.1	6.3

Table 3: Memory requirements for each scheme implementation. (cont.)

Scheme	impl.	code	data	bss	keygen	sign	verify
ov-1p-pkc-skc	ref	29467	0	0	247.6	247.5	277.9
	m4fspeed	119175	0	0	371.1	237.4	274.4
	m4fstack	119103	0	0	371.1	237.4	6.3
tuov_ip	ref	92760	0	0	3201.4	3517.0	1764.9
tuov_ip_pkc	ref	88400	0	0	502.6	15.7	401.6
tuov_ip_pkc_skc	ref	88448	0	0	736.4	800.5	401.6
tuov_is	ref	49316	0	0	337.6	10.6	1.6
tuov_is_pkc	ref	49504	0	0	740.1	10.6	595.6
tuov_is_pkc_skc	ref	49548	0	0	1082.1	1179.2	595.6
tuov_iii	ref	92576	0	0	981.0	24.0	5.8
tuov_iii_pkc	ref	92712	0	0	2177.7	24.0	1764.9
tuov_iii_pkc_skc	ref	92760	0	0	3201.4	3517.0	1764.9
tuov_v_pkc	ref	86304	0	0	unable to test		
tuov_v_pkc_skc	ref	86352	0	0	unable to test		
snova-24-5-16-4-esk	ref	52132	0	336	165.0	87.9	115.4
snova-24-5-16-4-ssk	ref	52132	0	336	165.0	165.1	115.4
snova-25-8-16-3-esk	ref	28240	0	299	186.2	85.4	119.8
snova-25-8-16-3-ssk	ref	28240	0	299	186.2	186.3	119.8
snova-28-17-16-2-esk	ref	16436	0	280	302.0	124.2	195.0
snova-28-17-16-2-ssk	ref	16436	0	280	302.0	302.1	195.0
snova-37-8-16-4-esk	ref	52440	0	336	625.3	289.1	401.8
snova-37-8-16-4-ssk	ref	52440	0	336	625.3	625.4	401.8
snova-43-25-16-2-esk	ref	15060	0	280	1015.1	407.9	650.6
snova-43-25-16-2-ssk	ref	15060	0	280	1015.1	1015.2	650.6
snova-49-11-16-3-esk	ref	26912	0	299	852.6	361.6	528.0
snova-49-11-16-3-ssk	ref	26912	0	299	852.6	852.7	528.0
snova-60-10-16-4-esk	ref	52588	0	336	1897.8	820.3	1179.7
snova-60-10-16-4-ssk	ref	52588	0	336	1897.8	1897.9	1179.7
snova-61-33-16-2-esk	ref	15020	0	280	2581.5	1027.9	1643.0
snova-61-33-16-2-ssk	ref	15020	0	280	2581.5	2581.6	1643.0
snova-66-15-16-3-esk	ref	27624	0	299	2117.3	876.1	1297.9
snova-66-15-16-3-ssk	ref	27624	0	299	2117.3	2117.4	1297.9

Table 3: Memory requirements for each scheme implementation. (cont.)

Scheme	impl.	code	data	bss	keygen	sign	verify
cross-sha2-r-sdp-1-fast	ref	14244	0	104	5.1	213.2	103.1
cross-sha2-r-sdp-1-small	ref	15285	0	104	5.1	691.1	314.9
cross-sha2-r-sdp-3-fast	ref	14744	0	128	9.7	317.2	154.4
cross-sha2-r-sdp-3-small	ref	14921	0	128	9.7	1238.9	584.9
cross-sha2-r-sdp-5-fast	ref	14580	0	152	16.4	839.3	401.1
cross-sha2-r-sdp-5-small	ref	14657	0	152	16.4	1661.8	784.1
cross-sha2-r-sdpg-1-fast	ref	18409	0	104	2.7	127.8	67.9
cross-sha2-r-sdpg-1-small	ref	18674	0	104	2.7	455.4	239.7
cross-sha2-r-sdpg-3-fast	ref	19609	0	128	4.4	200.3	105.9
cross-sha2-r-sdpg-3-small	ref	19994	0	128	4.4	737.1	383.9
cross-sha2-r-sdpg-5-fast	ref	18669	0	152	7.2	389.2	208.7
cross-sha2-r-sdpg-5-small	ref	18818	0	152	7.2	1004.5	521.6
cross-sha3-r-sdp-1-fast	ref	14472	0	208	4.6	213.3	103.1
cross-sha3-r-sdp-1-small	ref	15353	0	208	4.6	691.2	314.9
cross-sha3-r-sdp-3-fast	ref	14884	0	208	9.1	317.1	154.1
cross-sha3-r-sdp-3-small	ref	14825	0	208	9.1	1238.9	584.6
cross-sha3-r-sdp-5-fast	ref	14576	0	208	15.8	839.3	400.7
cross-sha3-r-sdp-5-small	ref	14629	0	208	15.8	1661.9	783.7
cross-sha3-r-sdpg-1-fast	ref	18605	0	208	2.3	127.9	67.9
cross-sha3-r-sdpg-1-small	ref	18846	0	208	2.3	455.5	239.8
cross-sha3-r-sdpg-3-fast	ref	19689	0	208	3.9	200.3	105.6
cross-sha3-r-sdpg-3-small	ref	19846	0	208	3.9	737.2	383.6
cross-sha3-r-sdpg-5-fast	ref	18593	0	208	6.7	389.3	208.3
cross-sha3-r-sdpg-5-small	ref	18762	0	208	6.7	1004.5	521.2
meds9923	ref	16720	0	0	36.8	973.8	98.1
meds13220	ref	16844	0	0	43.0	176.1	46.6
meds134180	ref	9180	0	0	392.5	853.4	375.7
meds167717	ref	9152	0	0	448.7	567.0	420.3
meds41711	ref	8948	0	0	135.6	1268.2	172.2
meds55604	ref	9012	0	0	158.3	383.6	156.5
aimer-l1-param1	ref	19302	468	0	10.7	183.2	192.1
aimer-l1-param2	ref	19894	468	0	10.7	432.2	441.1

Table 3: Memory requirements for each scheme implementation. (cont.)

Scheme	impl.	code	data	bss	keygen	sign	verify
aimer-11-param3	ref	19658	468	0	10.7	1390.4	1399.3
aimer-13-param1	ref	23398	468	0	23.3	404.1	425.4
aimer-13-param2	ref	23570	468	0	23.3	1027.7	1049.0
aimer-15-param1	ref	28142	468	0	57.0	821.4	876.1
aimer-15-param2	ref	28490	468	0	57.0	2035.7	2090.4
mqom_cat1_gf251_fast	ref	16865	0	0	180.0	390.0	246.7
mqom_cat1_gf251_short	ref	18193	0	0	180.0	649.8	371.0
mqom_cat1_gf31_fast	ref	23718	0	0	256.7	598.5	411.6
mqom_cat1_gf31_short	ref	23510	0	0	256.7	847.8	541.1
mqom_cat3_gf251_fast	ref	17074	0	0	665.0	1254.4	803.1
mqom_cat3_gf251_short	ref	18710	0	0	665.0	1840.4	1116.9
mqom_cat3_gf31_fast	ref	23881	0	0	952.0	2099.4	1500.2
mqom_cat3_gf31_short	ref	24025	0	0	952.0	2606.9	1732.4
mqom_cat5_gf251_fast	ref	20401	0	0	1662.4	3146.7	2115.1
mqom_cat5_gf251_short	ref	20137	0	0	1662.4	4019.1	2477.9
mirith_Ia_fast	ref	7610	256	0	10.0	119.6	22.2
mirith_Ia_short	ref	7635	256	0	10.0	986.7	92.1
mirith_Ib_fast	ref	7602	256	0	18.7	147.5	32.9
mirith_Ib_short	ref	7675	256	0	18.7	1156.7	117.1
mirith_IIIa_fast	ref	7720	256	0	21.4	260.2	45.0
mirith_IIIa_short	ref	7889	256	0	21.4	2130.0	139.8
mirith_IIIb_fast	ref	7760	256	0	32.1	291.2	57.7
mirith_IIIb_short	ref	7901	256	0	32.1	2314.5	162.3
mirith_Va_fast	ref	7890	256	0	44.0	473.1	83.2
mirith_Va_short	ref	7987	256	0	44.0	3701.9	202.5
mirith_Vb_fast	ref	7914	256	0	61.4	522.6	103.5
mirith_Vb_short	ref	7991	256	0	61.4	3994.6	234.9
mirith_hypercube_Ia_fast	ref	8844	256	0	10.0	75.1	20.4
	opt	10932	0	0	10.0	75.1	20.4
mirith_hypercube_Ia_short	ref	8781	256	0	10.0	212.5	30.4
mirith_hypercube_Ia_shorter	ref	8843	256	0	10.0	1728.9	211.2

Table 3: Memory requirements for each scheme implementation. (cont.)

Scheme	impl.	code	data	bss	keygen	sign	verify
mirith_hypercube_Ib_fast	ref	8820	256	0	18.7	94.7	30.5
	opt	10908	0	0	18.7	94.7	30.5
mirith_hypercube_Ib_short	ref	8825	256	0	18.7	231.8	40.2
mirith_hypercube_Ib_shorter	ref	8819	256	0	18.7	1748.7	221.0
mirith_hypercube_IIIa_fast	ref	8966	256	0	21.4	163.1	41.6
mirith_hypercube_IIIa_short	ref	9139	256	0	21.4	475.0	55.2
mirith_hypercube_IIIa_shorter	ref	9109	256	0	21.4	3788.1	325.9
mirith_hypercube_IIIb_fast	ref	9002	256	0	32.1	185.1	53.8
mirith_hypercube_IIIb_short	ref	9159	256	0	32.1	497.1	67.0
mirith_hypercube_IIIb_shorter	ref	9093	256	0	32.1	3809.8	337.6
mirith_hypercube_Va_fast	ref	9140	256	0	44.0	301.2	79.2
mirith_hypercube_Va_short	ref	9241	256	0	44.0	832.8	93.8
mirith_hypercube_Va_shorter	ref	9203	256	0	unable to test		
mirith_hypercube_Vb_fast	ref	9160	256	0	61.4	336.8	98.8
mirith_hypercube_Vb_short	ref	9245	256	0	61.4	868.6	112.8
mirith_hypercube_Vb_shorter	ref	9247	256	0	unable to test		
perk-128-fast-3	ref	11053	4	0	7.5	306.0	305.8
	m4	13421	4	0	7.5	23.5	20.2
perk-128-fast-5	ref	11129	4	0	8.8	298.5	298.3
	m4	13493	4	0	8.8	24.6	21.2
perk-128-short-3	ref	31757	4	0	7.5	1524.5	1524.3
	m4	26313	4	0	7.5	27.1	24.6
perk-128-short-5	ref	31905	4	0	8.8	1428.5	1428.3
	m4	26461	4	0	8.8	27.9	25.4
perk-192-fast-3	ref	11377	4	0	14.6	670.5	670.2
	m4	12253	4	0	14.6	46.6	40.4
perk-192-fast-5	ref	11365	4	0	16.5	646.7	646.4
	m4	12277	4	0	16.5	47.6	41.4
perk-192-short-3	ref	31789	4	0	14.6	3388.5	3388.2
	m4	24189	4	0	14.6	50.1	45.6
perk-192-short-5	ref	31813	4	0	16.5	3148.5	3148.2
	m4	24913	4	0	16.5	50.7	46.1

Table 3: Memory requirements for each scheme implementation. (cont.)

Scheme	impl.	code	data	bss	keygen	sign	verify
perk-256-fast-3	ref	11313	4	0	24.9	1163.9	1163.7
	m4	12337	4	0	24.9	78.4	68.3
perk-256-fast-5	ref	11325	4	0	27.4	1114.5	1114.1
	m4	12337	4	0	27.4	79.0	69.0
perk-256-short-3	ref	31961	4	0	unable to test		
	m4	31905	4	0	24.9	80.3	73.0
perk-256-short-5	ref	31973	4	0	unable to test		
	m4	32989	4	0	27.4	80.1	73.1
ascon-sign-128f-robust	ref	17664	0	0	3.1	2.7	2.9
ascon-sign-128f-simple	ref	17596	0	0	2.6	2.1	2.4
ascon-sign-128s-robust	ref	17972	0	0	3.3	2.7	2.2
ascon-sign-128s-simple	ref	17904	0	0	2.8	2.2	1.7
ascon-sign-192f-robust	ref	17960	0	0	5.9	4.8	4.4
ascon-sign-192f-simple	ref	17912	0	0	4.7	3.6	3.6
ascon-sign-192s-robust	ref	18472	0	0	6.2	4.9	4.2
ascon-sign-192s-simple	ref	18424	0	0	5.0	3.7	3.0
sphincs-a-sha2-128f	ref	6343	0	0	274.6	274.1	274.1
sphincs-a-sha2-128s	ref	6899	0	0	572.2	571.9	571.6
sphincs-a-sha2-192f	ref	6867	0	0	492.3	490.7	490.6
sphincs-a-sha2-192s	ref	7423	0	0	1259.2	1258.4	1258.0
sphincs-a-sha2-256f	ref	7203	0	0	1046.7	1044.6	1044.3
sphincs-a-sha2-256s	ref	7511	0	0	2208.4	2207.1	2206.7
sphincs-a-shake-128f	ref	5552	0	0	274.5	274.0	274.0
sphincs-a-shake-128s	ref	6108	0	0	572.2	571.8	571.5
sphincs-a-shake-192f	ref	5916	0	0	491.7	490.2	490.1
sphincs-a-shake-192s	ref	6428	0	0	1258.6	1257.8	1257.5
sphincs-a-shake-256f	ref	6188	0	0	1046.2	1044.1	1043.8
sphincs-a-shake-256s	ref	6456	0	0	2207.9	2206.5	2206.2

## References

- AAC<sup>+</sup>23. Muhammad Rezal Kamel Ariffin, Nur Azman Abu, Terry Lau Shue Chien, Zahari Mahad, Amir Hamzah Abd Ghafar, and Nurul Amiera Sakinah Abdul Jamal. KAZ-SIGN, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9

- AAS<sup>+</sup>19. Gorjan Alagic, , Jacob Alperin-Sheriff, Daniel Apon, David Cooper, Quynh Dang, Yi-Kai Liu, Carl Miller, Dustin Moody, Rene Peralta, Ray Perlner, Angela Robinson, and Daniel Smith-Tone. NISTIR8240 – status report on the first round of the nist post-quantum cryptography standardization process. January 2019. <https://doi.org/10.6028/NIST.IR.8240>. 1
- AASA<sup>+</sup>20. Gorjan Alagic, Jacob Alperin-Sheriff, Daniel Apon, David Cooper, Quynh Dang, John Kelsey, Yi-Kai Liu, Carl Miller, Dustin Moody, Rene Peralta, Ray Perlner, Angela Robinson, and Daniel Smith-Tone. NISTIR8309 – status report on the second round of the nist post-quantum cryptography standardization process, July 2020. <https://doi.org/10.6028/NIST.IR.8309>. 2
- ABB<sup>+</sup>23a. Najwa Aaraj, Slim Bettaieb, Loïc Bidoux, Alessandro Budroni, Victor Dyseryn, Andre Esser, Philippe Gaborit, Mukul Kulkarni, Victor Mateu, Marco Palumbi, Lucas Perin, and Jean-Pierre Tillich. PERK, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- ABB<sup>+</sup>23b. Nicolas Aragon, Magali Bardet, Loïc Bidoux, Jesús-Javier Chi-Domínguez, Victor Dyseryn, Thibault Feneuil, Philippe Gaborit, Antoine Joux, Matthieu Rivain, Jean-Pierre Tillich, and Adrien Vinçotte. RYDE, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 4, 5, 7
- ABB<sup>+</sup>23c. Nicolas Aragon, Magali Bardet, Loïc Bidoux, Jesús-Javier Chi-Domínguez, Victor Dyseryn, Thibault Feneuil, Philippe Gaborit, Romaric Neveu, Matthieu Rivain, and Jean-Pierre Tillich. MIRA, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 4, 5, 7
- AP20. Alexandre Adomnicai and Thomas Peyrin. Fixslicing AES-like ciphers: New bitsliced AES speed records on ARM-Cortex M and RISC-V. *IACR Transactions on Cryptographic Hardware and Embedded Systems*, 2021(1):402–425, Dec. 2020. <https://tches.iacr.org/index.php/TCHES/article/view/8739>. 3
- ARZV<sup>+</sup>23. Gora Adj, Luis Rivera-Zamarripa, Javier Verbel, Emanuele Bellini, Stefano Barbero, Andre Esser, Carlo Sanna, and Floyd Zweydinger. MiRitH, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- BBB<sup>+</sup>23a. Marco Baldi, Alessandro Barengi, Luke Beckwith, Jean-François Biasse, Andre Esser, Kris Gaj, Kamyar Mohajerani, Gerardo Pelosi, Edoardo Persichetti, Markku-Juhani O. Saarinen, Paolo Santini, and Robert Wallace. LESS, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- BBB<sup>+</sup>23b. Marco Baldi, Alessandro Barengi, Sebastian Bitzer, Patrick Karl, Felice Manganiello, Alessio Pavoni, Gerardo Pelosi, Paolo Santini, Jonas Schupp, Freeman Slaughter, Antonia Wachter-Zeh, and Violetta Weger. CROSS, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 4, 5
- BBB<sup>+</sup>24. Slim Bettaieb, Loïc Bidoux, Alessandro Budroni, Marco Palumbi, and Lucas Pandolfo Perin. Enabling perk on resource-constrained devices. *Cryptology ePrint Archive*, Paper 2024/088, 2024. <https://eprint.iacr.org/2024/088>. 7
- BBD<sup>+</sup>23. Joppe W. Bos, Olivier Bronchain, Léo Ducas, Serge Fehr, Yu-Hsuan Huang, Thomas Pornin, Eamonn W. Postlethwaite, Thomas Prest, Ludo N. Pulles, and Wessel van Woerden. HAWK, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- BBdSG<sup>+</sup>23. Carsten Baum, Lennart Braun, Cyprien Delpech de Saint Guilhem, Michael Kloöß, Christian Majenz, Shibam Mukherjee, Emmanuela Orsini, Sebastian Ramacher, Christian Rechberger, Lawrence Roy, and Peter Scholl. FAEST, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 4, 5, 9
- BCC<sup>+</sup>22. Daniel J. Bernstein, Tung Chou, Carlos Cid, Jan Gilcher, Tanja Lange, Varun Maram, Ingo von Maurich, Rafael Misoczki, Ruben Niederhagen, Edoardo Persichetti, Christiane Peters, Nicolas Sendrier, Jakub Szefer, Cen Jung Tjhai, Martin Tomlinson, and Wen Wang. Classic McEliece. Technical report, National Institute of Standards and Technology, 2022. available at <https://csrc.nist.gov/projects/post-quantum-cryptography/round-4-submissions>. 1
- BCC<sup>+</sup>23a. Gustavo Banegas, Kévin Carrier, André Chailloux, Alain Couvreur, Thomas Debris-Alazard, Philippe Gaborit, Pierre Karpman, Johanna Loyer, Ruben Niederhagen, Nicolas Sendrier, Benjamin Smith, and Jean-Pierre Tillich. Wave, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- BCC<sup>+</sup>23b. Ward Beullens, Fabio Campos, Sofia Celi, Basil Hess, and Matthias J. Kannwischer. MAYO, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- BCC<sup>+</sup>23c. Ward Beullens, Fabio Campos, Sofia Celi, Basil Hess, and Matthias J. Kannwischer. Nibbling MAYO: Optimized implementations for AVX2 and Cortex-M4. *Cryptology ePrint Archive*, Paper 2023/1683, 2023. <https://eprint.iacr.org/2023/1683>. 8
- BCD<sup>+</sup>23. Ward Beullens, Ming-Shing Chen, Jintai Ding, Boru Gong, Matthias J. Kannwischer, Jacques Patarin, Bo-Yuan Peng, Dieter Schmidt, Cheng-Jih Shih, Chengdong Tao, and Bo-Yin Yang. UOV, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8

- BCH<sup>+</sup>23. Ward Beullens, Ming-Shing Chen, Shih-Hao Hung, Matthias J. Kannwischer, Bo-Yuan Peng, Cheng-Jih Shih, and Bo-Yin Yang. Oil and vinegar: Modern parameters and implementations. *IACR Transactions on Cryptographic Hardware and Embedded Systems*, 2023(3):321–365, Jun. 2023. 8
- BDN<sup>+</sup>23. Markus Bläser, Dung Hoang Duong, Anand Kumar Narayanan, Thomas Plantard, Youming Qiao, Arnaud Sipasseuth, and Gang Tang. ALTEQ, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9
- BKPV23. Luk Bettale, Delaram Kahrobaei, Ludovic Perret, and Javier Verbel. Biscuit, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- CCC<sup>+</sup>23. Ming-Shing Chen, Yu-Shian Chen, Chen-Mou Cheng, Shiuan Fu, Wei-Chih Hong, Jen-Hsuan Hsiang, Sheng-Te Hu, Po-Chun Kuo, Wei-Bin Lee, Feng-Hao Liu, and Justin Thaler. Preon, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9
- CCD<sup>+</sup>23a. Jung Hee Cheon, Hyeongmin Choe, Julien Devevey, Tim Güneysu, Dongyeon Hong, Markus Krausz, Georg Land, Marc Möller, Damien Stehlé, and MinJune Yi. Haetae: Shorter lattice-based fiat-shamir signatures. *Cryptology ePrint Archive*, Paper 2023/624, 2023. <https://eprint.iacr.org/2023/624>. 6
- CCD<sup>+</sup>23b. Jung Hee Cheon, Hyeongmin Choe, Julien Devevey, Tim Güneysu, Dongyeon Hong, Markus Krausz, Georg Land, Junbum Shin, Damien Stehlé, and MinJune Yi. HAETAE, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- CNL<sup>+</sup>23. Jinkyu Cho, Jong-Seon No, Yongwoo Lee, Young-Sik Kim, and Zahyun Koo. Enhanced pqsigRM, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- CNP<sup>+</sup>23. Tung Chou, Ruben Niederhagen, Edoardo Persichetti, Lars Ran, Tovohery Hajatiana Randrianarisoa, Krijn Reijnders, Simona Samardjiska, and Monika Trimoska. MEDS, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- CSSF<sup>+</sup>23. Jorge Chavez-Saab, Maria Corte-Real Santos, Luca De Feo, Jonathan Komada Eriksen, Basil Hess, David Kohel, Antonin Leroux, Patrick Longa, Michael Meyer, Lorenz Panny, Sikhar Patranabis, Christophe Petit, Francisco Rodríguez Henríquez, Sina Schaeffler, and Benjamin Wesolowski. SQISign, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- DGG<sup>+</sup>23. Jintai Ding, Boru Gong, Hao Guo, Xiaou He, Yi Jin, Yuansheng Pan, Dieter Schmidt, Chengdong Tao, Danli Xie, Bo-Yin Yang, and Ziyu Zhao. TUOV, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- dPEK<sup>+</sup>23. Rafael del Pino, Thomas Espitau, Shuichi Katsumata, Mary Maller, Fabrice Mouhartem, Thomas Prest, Mélissa Rossi, and Markku-Juhani Saarienen. Raccoon, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- ENST23. Thomas Espitau, Guilhem Niot, Chao Sun, and Mehdi Tibouchi. SQUIRRELS, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- FI23. Hiroki Furue and Yasuhiko Ikematsu. A new security analysis against MAYO and QR-UOV using rectangular minrank attack. In Junji Shikata and Hiroki Kuzuno, editors, *Advances in Information and Computer Security - 18th International Workshop on Security, IWSEC 2023, Yokohama, Japan, August 29-31, 2023, Proceedings*, volume 14128 of *Lecture Notes in Computer Science*, pages 101–116. Springer, 2023. 9
- FIH<sup>+</sup>23. Hiroki Furue, Yasuhiko Ikematsu, Fumitaka Hoshino, Tsuyoshi Takagi, Kan Yasuda, Toshiyuki Miyazawa, Tsunekazu Saito, and Akira Nagai. QR-UOV, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- FR23. Thibault Feneuil and Matthieu Rivain. MQOM, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- GCF<sup>+</sup>23. Louis Goubin, Benoît Cogliati, Jean-Charles Faugère, Pierre-Alain Fouque, Robin Larrieu, Gilles Macario-Rat, Brice Minaud, and Jacques Patarin. PROV, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- HBD<sup>+</sup>19. Andreas Hulsing, Daniel J. Bernstein, Christoph Dobraunig, Maria Eichlseder, Scott Fluhrer, Stefan-Lukas Gazdag, Panos Kampanakis, Stefan Kolbl, Tanja Lange, Martin M Lauridsen, Florian Mendel, Ruben Niederhagen, Christian Rechberger, Joost Rijneveld, Peter Schwabe, and Jean-Philippe Aumasson. SPHINCS+. Technical report, National Institute of Standards and Technology, 2019. available at <https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions>. 1
- IA24. Yasuhiko Ikematsu and Rika Akiyama. Revisiting the security analysis of snova. *Cryptology ePrint Archive*, Paper 2024/096, 2024. <https://eprint.iacr.org/2024/096>. 8
- KCC<sup>+</sup>23. Seongkwang Kim, Jihoon Cho, Mingyu Cho, Jincheol Ha, Jihoon Kwon, Byeonghak Lee, Joohee Lee, Jooyoung Lee, Sangyub Lee, Dukjae Moon, Mincheol Son, and Hoyjin Yoon. AIMER, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9
- KRSS19. Matthias J. Kannwischer, Joost Rijneveld, Peter Schwabe, and Ko Stoffelen. pqm4: Testing and benchmarking nist pqc on arm cortex-m4. *Cryptology ePrint Archive*, Paper 2019/844, 2019. <https://eprint.iacr.org/2019/844>. 2

- KSSW22. Matthias J. Kannwischer, Peter Schwabe, Douglas Stebila, and Thom Wiggers. Improving software quality in cryptography standardization projects. In *IEEE European Symposium on Security and Privacy, EuroS&P 2022 - Workshops, Genoa, Italy, June 6-10, 2022*, pages 19–30, Los Alamitos, CA, USA, 2022. IEEE Computer Society. 2
- LA23. Ignacio Luengo and Martín Avendaño. DME-Sign, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- LDK<sup>+</sup>19. Vadim Lyubashevsky, Léo Ducas, Eike Kiltz, Tancrede Lepoint, Peter Schwabe, Gregor Seiler, and Damien Stehlé. CRYSTALS-DILITHIUM. Technical report, National Institute of Standards and Technology, 2019. available at <https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions>. 1
- LZ23. Dongxi Liu and Raymond K. Zhao. eMLE-Sig 2.0, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9
- MFG<sup>+</sup>23. Carlos Aguilar Melchor, Thibault Feneuil, Nicolas Gama, Shay Gueron, James Howe, David Joseph, Antoine Joux, Edoardo Persichetti, Tovohery H. Randrianarisoa, Matthieu Rivain, and Dongze Yue. SDitH, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7
- MRPC<sup>+</sup>23. Gilles Macario-Rat, Jacques Patarin, Benoit Cogliati, Jean-Charles Faugère, Pierre-Alain Fouque, Louis Gouin, Robin Larrieu, and Brice Minaud. Rectangular attack on vox. Cryptology ePrint Archive, Paper 2023/1822, 2023. <https://eprint.iacr.org/2023/1822>. 9
- NIS23a. Post-quantum cryptography: Digital signature schemes, 2023. Available at <https://csrc.nist.gov/Projects/pqc-dig-sig/round-1-additional-signatures>. 1, 19, 20, 21, 22
- NIS23b. Post-quantum cryptography: Round 4 submissions, 2023. Available at <https://csrc.nist.gov/Projects/post-quantum-cryptography/round-4-submissions>. 1
- NP23. Jianfang "Danny" Niu and Daniel Enrique Nágler Piazuolo. Xifrat1-Sign.I, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 10
- PCF<sup>+</sup>23. Jacques Patarin, Benoît Cogliati, Jean-Charles Faugère, Pierre-Alain Fouque, Louis Goubin, Robin Larrieu, Gilles Macario-Rat, and Brice Minaud. VOX, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9
- PFH<sup>+</sup>19. Thomas Prest, Pierre-Alain Fouque, Jeffrey Hoffstein, Paul Kirchner, Vadim Lyubashevsky, Thomas Pornin, Thomas Ricosset, Gregor Seiler, William Whyte, and Zhenfei Zhang. Falcon. Technical report, National Institute of Standards and Technology, 2019. available at <https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions>. 1
- RBK<sup>+</sup>23. Stefan Ritterhoff, Sebastian Bitzer, Patrick Karl, Georg Maringer, Thomas Schamberger, Jonas Schupp, Georg Sigl, Antonia Wachter-Zeh, and Violetta Weger. FuLeeCa, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- Rod23a. Borja Gómez Rodríguez. 3WISE, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- Rod23b. Borja Gómez Rodríguez. HPPC, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- SAB<sup>+</sup>19. Peter Schwabe, Roberto Avanzi, Joppe Bos, Léo Ducas, Eike Kiltz, Tancrede Lepoint, Vadim Lyubashevsky, John M. Schanck, Gregor Seiler, and Damien Stehlé. CRYSTALS-KYBER. Technical report, National Institute of Standards and Technology, 2019. available at <https://csrc.nist.gov/projects/post-quantum-cryptography/round-2-submissions>. 1
- SF23. Igor Semaev and Martin Feussner. EHTv3 and EHTv4, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- SGJ<sup>+</sup>23. Vikas Srivastava, Naina Gupta, Arpan Jati, Anubhab Baksi, Jakub Breier, Anupam Chattopadhyay, Sumit Kumar Debnath, and Xiaolu Hou. Ascon-Sign, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9
- SHDS23. Djiby Sow, Abiodoun Clement Hounkpevi, Sidoine Djimnaibeye, and Michel Seck. EagleSign, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 6
- SS17. Peter Schwabe and Ko Stoffelen. All the AES you need on Cortex-M3 and M4. In *Selected Areas in Cryptology – SAC 2016*, pages 180–194, 2017. <https://eprint.iacr.org/2016/714>. 3
- ST23. Daniel Smith-Tone. A total break of the 3wise digital signature scheme. Cryptology ePrint Archive, Paper 2023/1535, 2023. <https://eprint.iacr.org/2023/1535>. 8
- WCD<sup>+</sup>23. Lih-Chung Wang, Chun-Yen Chou, Jintai Ding, Yen-Liang Kuan, Ming-Siou Li, Bo-Shu Tseng, Po-En Tseng, and Chia-Chun Wang. SNOVA, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 8
- YCZ23. Yu Yu, Hongrui Cui, and Kaiyi Zhang. SPHINCS-alpha, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 9
- YJL<sup>+</sup>23. Yang Yu, Huiwen Jia, Leibo Li, Delong Ran, Zhiyuan Qiu, Shiduo Zhang, Xiuhan Lin, and Xiaoyun Wang. HuFu, 2023. Submission to the NIST Additional Digital Signature Scheme Project [NIS23a]. 5, 7